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18 October, 2021

ECe 3200-01 Lab 8

Common-Source (CS) and Common-Gate (CG) Small-Signal MOSFET

**Objective:**

The objective of this lab is to design the specification and test the characteristics performance of a CS and a CG amplifier.

**Prelab:**

1. In the amplifier circuit shown in fig.2 determine the circuit parameters R1, R2, RS and RD so that the DC quantities VG = 5.9 V, ID = 4 mA and VDS = 8 V are acquired. Also, the AC input impedance, Zin, in CS configuration is required to be Zin = 132 kΩ.
2. Draw the small signal mid band frequency equivalent circuit of the amplifier and determine a) the loaded voltage gain AV , b) the input impedance ZIn, and c) the output impedance Ro external to the load resistor RL = 100 kΩ, for CS and CG configurations.

Av = .. -61.. , Zin = ..130 kΩ…. Ro = …2.2 k……… ( CS) Calc.

Av = .. -61.. , Zin = ..34.1 Ω…. Ro = …2.2 k……… ( CG) //

**Procedure:**

1. Construct the circuit shown in fig. 2 in CS configuration, using “standard” resistors.
2. Measure the following DC values; values are the same regardless of CS or CG configurations.

Diagram, schematic

Description automatically generated

VG = 5.81 V , VS = 3.583 V , VD = 13.12V , (measured)

VDS = VD –VS = 9.537 V , ID = (VDD –VD )/ RS = 7.88 mA (derived)

1. Measure the mid-band AC quantities in both configurations.

A screenshot of a computer

Description automatically generated with medium confidence

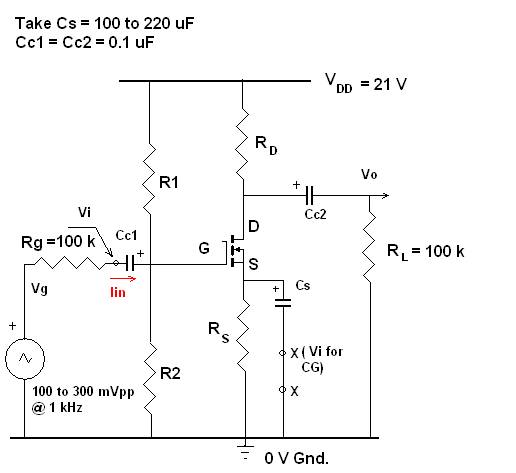
Av = -56.988 (loaded) , Zin = 203 kΩ Ro = 2.2 k (CS) Meas.

Av = + 57.2 (loaded) , Zin = 31.6 Ω Ro = 2.2 k (CG) //

Here AV = vo/vi and Zin = vi / Iin where Iin = (vg – vi)/ Rg .

To arrange the circuit into CG configuration insert the signal generator with Rg , across the new position marked X-X and **ground** the **negative** end of the capacitor CC1.

Fig.2 CS Amplifier



**NOTE**

**When amplifier is configured in CG position change Rg to, Rg = 390 Ω**

Diagram, schematic

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

**Calculations:**

Calc . & Design

From trace @ ID = 4 mA , VGS = 1.9 V VS = VG – VGS = 5.9 – 1.9 = 4 V

**RS = 4 V / 4 mA = 1.0 k Standard**

VD VS + VDS = 4 + 8 = 12 V → VRd = VDD –VD = 21 – 12 = 9 V

RD = 9 V / 4 mA = 2.25 k → **Standard RD = 2.2 k**

Divider design:

VG = R2 . VDD / ( R1 + R2 ) → 5.9 = 22 R1 / ( R1 + R 2 ) → R1 = 2.56 R2

Zin = R1 || R2 = R1 R2 / ( R1 + R2 ) → Zin = 0.719 R2 → 132 = 0.719 R2 → R2 = 183 k

**R2 = 180 k ….. Standard** . R1 = 2.56 x 183 = 468 k → **R1 = 470 k ….Standard**

**Small signal gm : Calc. From theory**

Kn = 0.1 A/V2 , VTh = 1.6 V Assumed FET parameters

gm = √ 2 Kn ID = √ 2 x 0.1x 4x10-3 = 28.28 mS

AV ( CS or CG ) = gm ( RD || RL ) = gm (2200 || 100,000 ) = 61

Zin ( CS ) = 180 k || 470 k = 130 k

Zin ( CG ) = ( 1/gm || RS ) = ( 1/ 28.28 x 10-3 || 1000 ) = ( 35.36 || 1000 ) = 34.1 Ω

**Modeling FET Mathematically:**

**Assume FET eqn. in saturation region follows the law , ID = Kn/2 ( VGS - VTh )2.**

From graph VTh = 1.6 V where ID = 0. Then take on point on the curve as ID = 8 mA at VGS = 2 V.

Substitute the values in the eqn. and solve for Kn.

0.008 = Kn / 2 ( 2 – 1.6 ) 2 → Kn = 0.1 A/V2

Note: ( if you take ID = 4 mA at VGS = 1.9 V the value of Kn will be 0.09 mA/ V2 making an insignificant difference in the overall calculation).

**Analysis:**

Percent Error

VG (% error) = 0%, VDS (% error) = 25.5%, ID (% error) = 88.55

When comparing the measurements found in the procedure, and the calculated values, we can see that there is a significant % error between the VDS and ID values. This is due to the different MOSFET transistor used than the ones stated in the lab manual. In this Pspice simulation, the VN2222LM MOSFET was used transistor instead of the VN0106.

**Conclusion:**

As a result of this lab, I was able to better understand how to make measurements of the small-signal frequency response of a MOSFET both in CG and CS configuration. I was also able to observe the Miller Effect applied on the circuit. Although I was not able perform the lab physically, I was still able to visualize and understand the circuit with the help of pSpice, and the zoom meeting provided. Through the lab, we can see that the voltage gain of a CE amplifier varies with the frequency. An emitter bypass capacitor is in parallel with RE to provide low reactance to the AC signal for DC measurements. The reactance of the coupling capacitor is relatively high, thus small parts of the signal will pass from the amplifier stage to the load. As a result, CE cannot shunt the RE because of its large reactance at low signal frequencies. This would cause a drop off voltage gain at lower frequencies, similar to a high-pass frequency.